AMENDMENT TRANSMITTAL LETTER (Large Entity)

	Docket No.
Applicant(s): Shuichi Takayama et al.	NAK1-BG86

Serial No. 09/301,284	Filing Date August 28, 1999	Examiner T. Vo	Group Art Unit 2122

OIPE SP 2 5 2002 PATENT & TRADEMARK OFFICE (stamp)

Invention: **PROCESSOR FOR EXECUTING INSTRUCTION UNITS THAT ARE UNRELATED TO THE UNITS IN WHICH INSTRUCTIONS ARE READ AND A COMPILER, AN OPTIMIZATION APPARATUS, AN ASSEMBLER, A LINKER, A DEBUGGER, AND A DISASSEMBLER FOR SUCH A DEBUGGER**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

RECEIVED OCT 0 1 2002 Technology Center 2100

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	12	-	48	=	0	x $18.00	$0.00
INDEP. CLAIMS	2	-	11	=	0	x $84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

☒ No additional fee is required for amendment.
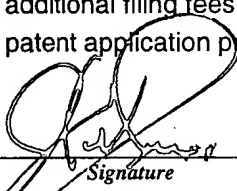
☐ Please charge Deposit Account No.   in the amount of
    A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $400.00 to cover the Request for Two Month Extension of Time Fee

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 16-2462
    A duplicate copy of this sheet is enclosed.

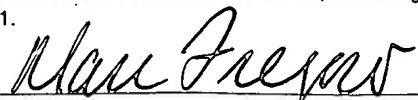   ☒   Any additional filing fees required under 37 C.F.R. 1.16.

    ☒   Any patent application processing fees under 37 CFR 1.17.

Dated: **September 20, 2002**

Signature

Joseph W. Price
Reg. No. 25,124
PRICE and GESS
2100 S.E. Main Street, Suite 250
Irvine, CA 92614
Tel: 949-261-8433

CC:

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE - GROUP 2122

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: T. Vo
Shuichi Takayama et al.	Group Art Unit: 2122
Serial No.: 09/301,284	
Filed: April 28, 1999	
For: PROCESSOR FOR EXECUTING INSTRUCTIONS IN UNITS THAT ARE UNRELATED TO THE UNITS IN WHICH INSTRUCTIONS ARE READ AND A COMPILER, AN OPTIMIZATION APPARATUS, AN ASSEMBLER, A LINKER, A DEBUGGER, AND A DISASSEMBLER FOR SUCH A DEBUGGER	Irvine, California 92614
	September 20, 2002

RECEIVED

OCT 0 1 2002

Technology Center 2100

AMENDMENT

Honorable Assistant Commissioner for Patents
Box AF
Washington, D.C. 20231

Dear Sir:

In response to the Office Action mailed April 23, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice Amended) A processor for reading instructions from a memory according to a program counter, and for executing the read instruction,